R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawings as originally filed, for example, in FIGS. 3, 4 and 7 and in the specification as originally filed, for example, on page 17, lines 5-20, on page 18, line 3 through page 20, line 4, on page 28, line 2 through page 30, line 21, and on page 38, line 5 through page 41, line 10. As such, no new matter has ben introduced.

IN THE SPECIFICATION

The objection to the Abstract has been obviated by appropriate amendment and should be withdrawn.

The specification has been amended for consistency and to update references to related cases. No new matter has been introduced.

CLAIM OBJECTIONS

The objections to claims 11 and 16 have been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claim 17 under 35 U.S.C. §112, second paragraph, has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-12 and 14-20 under 35 U.S.C. §102(e) as being anticipated by Patel, et al. (U.S. Patent No. 6,332,215, hereinafter Patel) has been obviated by appropriate amendment and should be withdrawn.

Patel is directed to Java virtual machine hardware for RISC and CISC processors (Title).

In contrast, the present invention (claim 1) provides a processor, an extension stack and a translation circuit. The translator circuit is configured to implement a stack using one or more of the internal registers of the processor **and** the extension stack. Claims 17 and 18 include similar limitations. Patel does not disclose or suggest a translator circuit as presently claimed. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Specifically, assuming, *arguendo*, the JAVA stack 50 of Patel is similar to the presently claimed extension stack (as suggested on page 6, lines 1-2 of the Office Action and for which Applicants' representative does not necessarily agree), Patel does

not disclose or suggest each and every element of the presently claimed invention, arranged as in the claims. In particular, a Java stack of Patel is implemented in **either** a hardware stack **OR** a CPU associated register file. For example, Patel states:

> The Java registers are also stored in **the Java stack** which **can be implemented as the hardware Java stack 50 OR the Java stack can be stored into the CPU associated register file** (column 4, lines 19-22 of Patel, emphasis and capitalization added).

In contrast, the presently claimed invention provides a stack implemented as **one or more internal registers AND an extension stack**. Therefore, Patel does not disclose or suggest each and every element of the presently claimed invention, arranged as in the claims. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Claims 2-16 and 19-20 depend, either directly or indirectly, from claim 1 or claim 18 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference.

New claims 21-23 depend directly from either claim 1 or claim 18 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference.

Applicants' representative respectfully traverses the Examiner's suggestion on page 5, line 12-18 of the Office Action

that "it is inherent that the native instructions can access and control both the JVM registers (44 of FIG. 3) and the Java CPU registers (48 of FIG. 3)" because "the bytecode (second instruction set) is translated into native instructions (first instruction set) in order to be executed, and that the JVM hardware registers are updated after each bytecode is executed." Inherency requires certainty of results, not mere possibility. See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). The Office Action fails to present factual evidence or a convincing line of reasoning why one skilled in the art would consider the native instructions necessarily being able to access and control both the JVM registers 44 and the Java CPU registers 48 of Patel.

Specifically, Patel states:

> **The Java registers are also stored in the Java stack** which **can be implemented as the hardware Java stack 50** or the Java stack can be stored into the CPU associated register file (column 4, lines 19-22 of Patel, emphasis added).

Patel further states:

> The Java registers are a part of the Java Virtual Machine and should not be confused with the general registers 46 or 48 which are operated upon by the central processing unit 26 (column 4, lines 35-38 of Patel)..

Thus, Patel does not support the position taken in the Office Action that the native instructions necessarily are able to access and control both the JVM registers 44 and the Java CPU registers 48

of Patel.

Furthermore, Applicants' representative respectfully traverses the Examiner's suggestion on page 6, lines 3-8 of the Office Action that it is inherent that "in the updating of the top of stack pointer that data will be transferred between locations in the stack and the top of the stack pointer register" because "the internal registers are contained in the Java stack (50 of FIG. 3) and that the pointer to the top of the stack is held within the internal registers." Inherency requires certainty of results, not mere possibility. See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). The Office Action fails to factually establish or present a convincing line of reasoning why one skilled in the art would consider that updating the top of stack pointer would necessarily require data be transferred between locations in the stack and the top of the stack pointer register. Specifically, Patel provides that the Java stack 50 may be implemented in the internal CPU registers or in a hardware Java stack 50 rather than the internal registers being contained in the Java stack 50.

Furthermore, the Office Action fails to present an explanation of why updating a pointer to the top of stack would necessarily require that data be transferred from a location in the stack to the top of stack pointer register. For example, the top of stack pointer may simply be incremented or decremented depending

on the stack operation being performed. As such, Patel does not appear to provide the required certainty of results and therefore does not support the conclusion of inherency.

Furthermore, Applicants' representative respectfully traverses the Examiner's suggestion on page 7, lines 7-12 of the Office Action that "it is inherent that the push and pop operations will transfer data between the internal registers and the stack" because "the internal registers are contained in the Java stack (50 of FIG. 3)." Inherency requires certainty of results, not mere possibility. See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). The Office Action fails to factually establish or provide a convincing line of reasoning why one skilled in the art would consider the internal registers necessarily being contained in the Java stack 50 as stated in the Office Action. Specifically, Patel provides that the internal registers of the CPU may be used to implement the Java stack 50 OR the Java stack 50 may be implemented as a hardware stack. Since Patel states that the Java stack 50 can be implemented as a hardware stack, it follows that Patel does not appear to support the position taken in the Office Action that pop and push operations would necessarily involve the internal registers of the CPU. As such, Patel does not appear to provide the required certainty of results and therefore does not support the conclusion of inherency.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claim 13 under 35 U.S.C. §103(a) as being unpatentable over Patel in view of Tremblay, et al. (U.S. Patent No. 6,021,469, hereinafter Tremblay) has been obviated by appropriate amendment and should be withdrawn.

Claim 13 depends, either directly or indirectly, from claim 1 which is believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be allowable.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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